ABSTRACT OF THE DISCLOSURE

A shift scan chain includes logic circuit blocks 11 - 18 and scan registers 21 - 28 connected at stages succeeding them. The shift chain is divided into divisional chains including the scan registers 21 - 24 and the scan registers 25 - 28. In the test operation mode of a semiconductor integrated circuit, test input data TI are supplied in synchronism with a multiplied clock signal CKD at a frequency twice of that of a clock signal CK. The test input data TI are converted by a serial/parallel conversion circuit 40 into parallel data S41 and S42, which are respectively supplied to the head scan registers 21 and 25 of the corresponding divisional chains. The length of each divisional chains becomes 1/2, and a test time period can be shortened.